



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,453	07/13/2004	Kerry Bernstein	BUR920040024US1	4452
30449	7590	12/20/2005	EXAMINER	
SCHMEISER, OLSEN + WATTS			TAN, VIBOL	
3 LEAR JET LANE			ART UNIT	
SUITE 201			PAPER NUMBER	
LATHAM, NY 12110			2819	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/710,453

Applicant(s)

BERNSTEIN ET AL.

Examiner

Vibol Tan

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 01 December 2005.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-32 is/are pending in the application.  
4a) Of the above claim(s) 23-32 is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-4,6,7,9-12,14,15,17,18,20 and 21 is/are rejected.  
7) ☒ Claim(s) 5,8,13,16,19 and 22 is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4, 6, 7, 9-12, 14, 15, 17, 18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka (US 2002/0008999).

In claim 1, Hidaka teaches all claimed features an integrated circuit in Fig. 3A, comprising: one or more logic stages (cascading inverters), at least one of said logic stages having a predominantly high input state (logic 1 to the input of second and fourth inverters) or having a predominantly low input state; wherein said logic stages having said predominantly high input state (logic 1 to the input of second and fourth inverters), comprise one or more thin gate dielectric (Tox1=thin) PFETs and one or more thick gate dielectric (Tox2=thick) NFETs; and wherein said logic stages having said predominantly low input state (logic 0 to the input of first and third inverters), comprise one or more thick gate dielectric (Tox2) PFETs and one or more thin gate dielectric (Tox1) NFETs; with the exception of teaching the PFETs for the predominantly low input state having high threshold voltage with respect to a reference PFET and the NFETs for the predominantly low input state having low threshold voltage with respect to a reference NFET, and the PFETs for the predominantly high input state having low threshold voltage with respect to a reference PFET and the NFETs for the

Art Unit: 2819

predominantly high input state having high threshold voltage with respect to a reference NFET. However, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the threshold voltages of the PFETs and the NFETs, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the threshold voltages of the PFETs and the NFETs in the logic stages of Hidaka's circuit, to further reduce power consumption in the standby state by suppressing leakage current in the logic stages.

In claim 2, Hidaka further teaches circuit of claim 1, wherein: said logic stages (the second and fourth inverters) having said predominantly high input state (logic 1) comprise all thin gate dielectric (Tox1) PFETs and comprise all thick gate dielectric (Tox2) NFETs; and said logic stages (the first and third inverters) having said predominantly low input state (logic 0) comprise all thick gate dielectric (Tox2) PFETs and comprise all thin gate dielectric (Tox1); with the exception of teaching wherein PFETs for the predominantly low input state having high threshold voltage and the NFETs for the predominantly low input state having low threshold voltage, and the PFETs for the predominantly high input state having low threshold voltage and the NFETs for the predominantly high input state having high threshold voltage. However, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the threshold voltages of the PFETs and the NFETs, since it has been held that where the general

Art Unit: 2819

conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the threshold voltages of the PFETs and the NFETs in the logic stages of Hidaka's circuit, to further reduce power consumption in the standby state by suppressing leakage current in the logic stages.

In claims 3-4, Hidaka further teaches the circuit of claim 1, wherein: all of said logic stages have either a predominantly high input state (second and fourth inverter, each is high) or a predominantly low input state; and wherein logic stages having predominantly high input states are connected in series with logic stages having predominantly low input states, said logic stages having predominantly high input states alternating with logic stages having predominantly low input states (as seen in Fig. 3A).

In claim 6, Hidaka further teaches the circuit of claim 1, wherein said logic stages (first to fourth inverter stages) operate monotonically (sequences whose successive members either consistently increase or decrease but do not oscillate in relative value).

In claim 7, Hidaka further teaches the circuit of claim 1, wherein said logic stages comprise pulsed CMOS logic circuits (Fig. 3A is CMOS logic circuits), dynamic domino circuits or fuse evaluation circuits (only one of the limitations has to be met, since the "or" conjunction is recited in the claim).

In claim 9, Hidaka teaches in Fig. 3A, a method of reducing leakage current in a circuit comprising specifying a reference PFET (selecting a PFET) having a specified threshold voltage (threshold voltage for the selected PFET) and gate dielectric thickness

Art Unit: 2819

(thickness of a gate for the selected PFET) and a reference NFET (selecting a NFET) having a specified threshold voltage (threshold voltage for the selected NFET) and gate dielectric thickness (thickness of a gate for the selected NFET); providing said circuit, said circuit having one or more logic stages (as seen in Fig. 3A); connecting at least one of said logic stages to an input having a predominantly high input state (logic 1) or having a predominantly low input state (logic 0); wherein said logic stages (second and fourth inverters) connected to said input having said predominantly high input state (logic 1), comprise one or more thin gate dielectric (Tox1 is thin) PFETs and one or more thick gate dielectric (Tox2 is thick) NFETs; and wherein said logic stages (first and third inverters) connected to said input having said predominantly low input state (logic 0), comprise one or more thick gate dielectric (Tox2) PFETs and one or more thin gate dielectric (Tox1) NFETs; with the exception of teaching wherein PFETs for the predominantly low input state having high threshold voltage and the NFETs for the predominantly low input state having low threshold voltage, and the PFETs for the predominantly high input state having low threshold voltage and the NFETs for the predominantly high input state having high threshold voltage. However, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the threshold voltages of the PFETs and the NFETs, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the threshold voltages of the PFETs and the NFETs

in the logic stages of Hidaka's circuit, to further reduce power consumption in the standby state by suppressing leakage current in the logic stages.

In claim 10, Hidaka further teaches the method of claim 9, said logic stages (the second and fourth inverters) having said predominantly high input state (logic 1) comprise all thin gate dielectric (Tox1) PFETs and comprise all thick gate dielectric (Tox2) NFETs; and said logic stages (the first and third inverters) having said predominantly low input state (logic 0) comprise all thick gate dielectric (Tox2) PFETs and comprise all thin gate dielectric (Tox1); with the exception of teaching wherein PFETs for the predominantly low input state having high threshold voltage and the NFETs for the predominantly low input state having low threshold voltage, and the PFETs for the predominantly high input state having low threshold voltage and the NFETs for the predominantly high input state having high threshold voltage. However, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the threshold voltages of the PFETs and the NFETs, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the threshold voltages of the PFETs and the NFETs in the logic stages of Hidaka's circuit, to further reduce power consumption in the standby state by suppressing leakage current in the logic stages.

In claims 11 and 12, Hidaka further teaches, the method of claim 9 further including connecting all of said logic stages to either a predominantly high input state (second and

Art Unit: 2819

fourth inverter, each is high) or a predominantly low input state; and further including logic stages having predominantly high input states are connected in series with logic stages having predominantly low input states, said logic stages having predominantly high input states alternating with logic stages having predominantly low input states (as seen in Fig. 3A).

In claim 14, Hidaka further teaches the method of claim 9, further including operating said logic stages (first to fourth inverter stages) monotonically (sequences whose successive members either consistently increase or decrease but do not oscillate in relative value).

In claim 15, Hidaka further teaches the method of claim 9, wherein said logic stages comprise pulsed CMOS logic circuits (Fig. 3A is CMOS logic circuits), dynamic domino circuits or fuse evaluation circuits (only one of the limitations has to be met, since the "or" conjunction is recited in the claim).

Method claims 17, 18, 20 and 21 correspond to detailed logic circuitry already discussed in method claims 9, 10, 14 and 15.


3. Claims 5, 8, 13, 16, 19 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 23-32 are withdrawn from consideration.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
**VIBOL TAN**  
**PRIMARY EXAMINER**